REMARKS

I. Status of the Application

Claims 2, 4-7, 9, 10, 20, 21 and 23-32 are pending in this application. In the September 18, 2005 office action, the Examiner:

A. Objected claim to claim 2 for what amounts to be an inadvertent scrivener's error;

B. Rejected claims 2, 4, 6, 9, 10, 20, 21 and 25-27 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 6,697,362 to Akella et al. (hereinafter "Akella");

C. Rejected claim 5 under 35 U.S.C. § 103(a) as allegedly being obvious over Akella in view of U.S. Patent No. 5,684,752 to Mills et al. (hereinafter "Mills");

D. Deemed claims 7, 23, 24 and 28 allowable if rewritten in independent format; and

E. Allowed claims 29-32.

In this response, claim 2 has been amended to further particularly point out and distinctly claim the inventive subject matter. Applicants respectfully traverse the rejections of the claims in view of the foregoing amendments and the following remarks.

II. The Objection to Claim 2 Should be Withdrawn

The Examiner objected to claim 2 and required that the phrase "memory switch" be changed to "network switch". Claim 2 has been amended as required by the Examiner. As a consequence, it is respectfully submitted that the objection to claim 2 is moot and should be

withdrawn.

III. Claim 2 is Not Anticipated by Akella

Claim 2 stands rejected as allegedly being anticipated by Akella. Applicants have amended claim 2 in part to clarify that the claimed "memory controller maintains a record identifying which of the plurality of logical memory devices was last written to". Claim 2 thus recites an association of one of the logical memory devices as the last memory device written to. It is believed that the original claim was of the same scope, and that this amendment merely clarifies the claim.

A. The Present Invention

Claim 2, as amended, is directed to a system having a memory and a network switch. The memory includes a plurality of logical memory devices. The network switch is coupled to the memory and includes a memory controller. The switch is configured to sequentially write a first portion of received packet data to a first of the plurality of logical memory devices and to write a second portion of the packet data to a second of the plurality of logical memory devices and to write a third portion of the packet data to a third of the plurality of logical memory devices. The memory controller maintains a record identifying which of the plurality of logical memory devices was last written to.

As discussed above the record maintained by the memory controller does not merely include an address of various memory devices, one of which is the last written to. Instead, the record identifies *which* of the memory devices was last written to. Support for the amendment may be found in the claims as originally filed, and also in step 710 of Fig. 7 of the

Application as filed.

B. Akella Does Not Disclose Maintaining a Record of *Which* Memory Controller Was Last Written To

As correctly noted by the Examiner, Akella is directed to a network switch and also includes circuitry for splitting packets and storing the fragments in different memory devices. However, Akella fails to disclose or suggest a memory controller, or any other device, that "maintains a record identifying *which* of the plurality of logical memory devices was last written to". At best, Akella merely stores the various addresses at which each packet is stored after it has been divided into fragments. It is neither required nor obvious to keep track of which device was last written to.

In particular, the Examiner correctly notes that the main discussion in Akella relating to storing and fragmenting data packets occurs in columns 7 and 8. The text in those columns, however, does not describe storing fragments in multiple devices such that it would be necessary to maintain a record identifying which memory device was last written to. Specifically, Akella at column 7, line 55 to column 8, line 16 merely teaches that packet segments are provided to predetermined memory addresses. There is nothing to indicate that Akella's system requires knowledge of the last memory device that was written to. To the contrary, it merely seems as though memory is allocated to packet segments independent of which memory device was last written to. Accordingly, Akella does not teach or suggest that a memory control "maintains a record identifying which of the plurality of logical memory devices was last written to", as claimed.

In the rejection of claim 2, the Examiner stated that Akella teaches "the Table RAM maintains all the record of addresses for packet portions in the logical memory devices including the logical memory device that was last written to". (September 19, 2005 office action at p.3). In other words, the Examiner appears to contend that since the Table RAM stores *all* addresses, it must necessarily include the address for the logical memory device last written to. Applicants agree that, at least philosophically, storing or maintaining *all* memory addresses written to necessarily requires storing the last memory address written to, since *all* memory addresses includes the last one written to. However, mere storage of all addresses does not constituted *identifying which* of the memory devices was last written to.

Thus, it appears that the Examiner misapprehended claim 2. The amendments herein are intended to clarify the claim, but not to change its scope. Because Akella fails to teach or suggest each and every element of claim 2, it is respectfully submitted that the rejection of claim 2 is in error and should be withdrawn.

IV. Claims 4-6, 9 and 10

Claims 4, 6, 9 and 10 also stand rejected as allegedly being anticipated by Akella. Claim 5 stands rejected as allegedly being obvious over Akella and Mills. Claims 4-6, 9 and 10 depend from and incorporate all of the limitations of claim 2. The modification of Akella proposed by the Examiner does not address the deficiencies of Akella with regard to claim 2 discussed above. Accordingly, for at least the same reasons as those set forth above in connection with claim 2, it is respectfully submitted that the prior art rejections of claims 4-6, 9 and 10 should be withdrawn.

V. Claim 20

Claim 20 also stands rejected as allegedly being anticipated by Akella. Claim 20 includes a limitation directed to "determining at the network switch the logical memory device to which a portion of the first data packet was last written". The Examiner applied the same reasoning to the rejection of claim 20 as discussed above in connection with claim 1. Accordingly, with respect to this element, the Examiner stated that Akella teaches that "the Table RAM maintains all the record of addresses for packet portions in the logical memory devices including the logical memory device that was last written to" (September 18, 2005 office action at p.3).

As discussed above in connection with claim 2, the Examiner appears to allege that, because all addresses are maintained with the Table RAM of Akella, the last written to address or device must be among those maintained. However, maintaining all addresses in the Table RAM does not constitute *determining* the logical memory device that was last written to. Accordingly, even if the Examiner's statement of the teachings of Akella is correct, Akella does not teach or suggest "determining at the network switch the logical memory device to which a portion of the first data packet was last written", as recited in claim 20.

Because Akella does not teach or suggest each and every element of claim 20, it is respectfully submitted that the anticipation rejection of claim 20 should be withdrawn.

V. Claim 21

Claim 21 also stands rejected as allegedly being anticipated by Akella. Claim 21 depends from and incorporates all of the limitations of claim 20. Accordingly, for at least the

same reasons as those set forth above in connection with claim 20, it is respectfully submitted that the prior art rejection of claim 21 should be withdrawn.

VI. Claim 25 is Allowable

Claim 25 stands rejected as allegedly being anticipated by Akella. Claim 25 includes a limitation directed to "determining *which* of the plurality of logical memory devices was the *last* of the plurality of logical memory devices to which one of the plurality of first data packet portions was written". Thus, claim 25 includes a limitation similar to that of claim 2, discussed above. As discussed above, Akella fails to teach or suggest such a claim element.

In the detailed rejection of claim 25, the Examiner asserted that a particular portion of Akella teaches this method step. That portion is set forth below:

> ...pool 225 via memory switch 220, as will be explained now in more detail with reference to FIG. 6. Switch interface 30 detects the arrival of a given packet 250 in one of the RX queues 22-1 . . . 22-n associated with ports 210-1. . .210-n (step S10). Switch interface 30 determines, from address table 20, the range of memory addresses within memory pool 225 for storing the given packet 250 based on from which of the ports 210-1 . . . 2210-n the given packet 250 arrived (step S20). Switch interface 30 immediately forwards a copy of the packet 250 (assuming it is the first. . . .

(Col. 7, lines 31-40)(cited by the Examiner at p.5 of the September 18, 2005 office action). Applicants respectfully disagree that the above-quoted paragraph from Akella in any way discloses a step of determining which of the memory devices was last written to. This paragraph neither inherently nor expressly discloses such a step. Instead, the above quoted paragraph merely discusses determining "the range of memory addresses within the memory pool. . . for storing the given packet". Determining a range of addresses for one or more packet fragments is not the same as, nor does it inherently require, determining which address or device was the last that was written to.

Accordingly, contrary to the Examiner's assertion, Akella does not teach or suggest "*which* of the plurality of logical memory devices was the *last* of the plurality of logical memory devices to which one of the plurality of first data packet portions was written", as recited in claim 25. Because Akella does not teach or suggest each and every element of claim 25, it is respectfully submitted that the anticipation rejection of claim 25 should be withdrawn.

VII. Claims 26 and 27

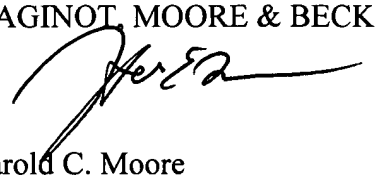
Claims 26 and 27 also stand rejected as allegedly anticipated by Akella. Claims 26 and 27 all depend from and incorporate all of the limitations of claim 25. As discussed above claim 20 is in a condition for allowance. As a consequence, for at least the same reasons as those set forth above in connection with claim 25, it is respectfully submitted that the prior art rejection of claims 26 and 27 should be withdrawn.

VIII. Conclusion

Applicant respectfully requests entry of the amendments and favorable consideration of the application. A prompt and favorable action on the merits is requested.

Respectfully Submitted,

MAGINOT, MOORE & BECK



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